AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1024] with the following replacement paragraph:

[1024] During typical SRAM operation, data is stored in a memory cell as a pair of true data and its complement, e.g., '1' and '0'. Before the read operation, both the BITLINE and BITLINE_L are precharged to VDD. When the memory cell is read, the true data, e.g., '1,' is connected to BITLINE and the ~~compliment~~ complement data, e.g., '0,' is connected to BITLINE_L. As a result, the voltage on BITLINE_L begins to fall while the voltage on BITLINE remains at VDD. When read column select 103 is enabled, BITLINE and BITLINE_L are connected to SA and ~~SA_I~~ SA_L respectively. The voltage difference transfers from BITLINE and BITLINE_L to SA and SA_L, respectively. When sense amplifier 120 is enabled, it senses and amplifies the small voltage/current difference between the SA and SA_L nodes.